```
NET "LCD_E"   LOC = "AB4" | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;
NET "LCD_RS"  LOC = "Y14" | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;
NET "LCD_RW"  LOC = "W13" | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;

NET "LCD_DB<7>" LOC = "Y15"  | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;
NET "LCD_DB<6>" LOC = "AB16" | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;
NET "LCD_DB<5>" LOC = "Y16"  | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;
NET "LCD_DB<4>" LOC = "AA12" | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;
NET "LCD_DB<3>" LOC = "AB12" | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;
NET "LCD_DB<2>" LOC = "AB17" | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;
NET "LCD_DB<1>" LOC = "AB18" | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;
NET "LCD_DB<0>" LOC = "Y13"  | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;
```

Figure 5-2: **UCF Location Constraints for the Character LCD**

LCD Controller

The 2 x 16 character LCD has an internal Sitronix ST7066U graphics controller that is functionally equivalent with the following devices.

- Samsung S6A0069X or KS0066U
- Hitachi HD44780
- SMOS SED1278

Memory Map

The controller has three internal memory regions, each with a specific purpose: DD RAM, CG ROM, and CG RAM. The display must be initialized before accessing any of these memory regions.

DD RAM

The Display Data RAM (DD RAM) stores the character code to be displayed on the screen. Most applications interact primarily with DD RAM. The character code stored in a DD RAM location references a specific character bitmap stored either in the predefined CG ROM character set or in the user-defined CG RAM character set.

Figure 5-3 shows the default address for the 32 character locations on the display. The upper line of characters is stored between addresses 0x00 and 0x0F. The second line of characters is stored between addresses 0x40 and 0x4F.

	Character Display Addresses																Undisplayed Addresses		
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	…	27
2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	…	67
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	…	40

Figure 5-3: **DD RAM Hexadecimal Addresses (No Display Shifting)**

Physically, there are 80 total character locations in DD RAM with 40 characters available per line. Locations 0x10 through 0x27 and 0x50 through 0x67 can be used to store other non-display data. Alternatively, these locations can also store characters that can only be displayed using controller's display shifting functions.

The Set DD RAM Address command initializes the address counter before reading or writing to DD RAM. Write DD RAM data using the Write Data to CG RAM or DD RAM command, and read DD RAM using the Read Data from CG RAM or DD RAM command.

The DD RAM address counter either remains constant after read or write operations, or auto-increments or auto-decrements by one location, as defined by the I/D set by the Entry Mode Set command.

CG ROM

The Character Generator ROM (CG ROM) contains the font bitmap for each of the predefined characters that the LCD screen can display, shown in Figure 5-4. The character code stored in DD RAM for each character location subsequently references a position with the CG ROM. For example, a hexadecimal character code of 0x53 stored in a DD RAM location displays the character 'S'. The upper nibble of 0x53 equates to DB[7:4] = 0101 binary and the lower nibble equates to DB[3:0] = 0011 binary. As shown in Figure 5-4, the character 'S' appears on the screen.

English/Roman characters are stored in CG ROM at their equivalent ASCII code addresses.

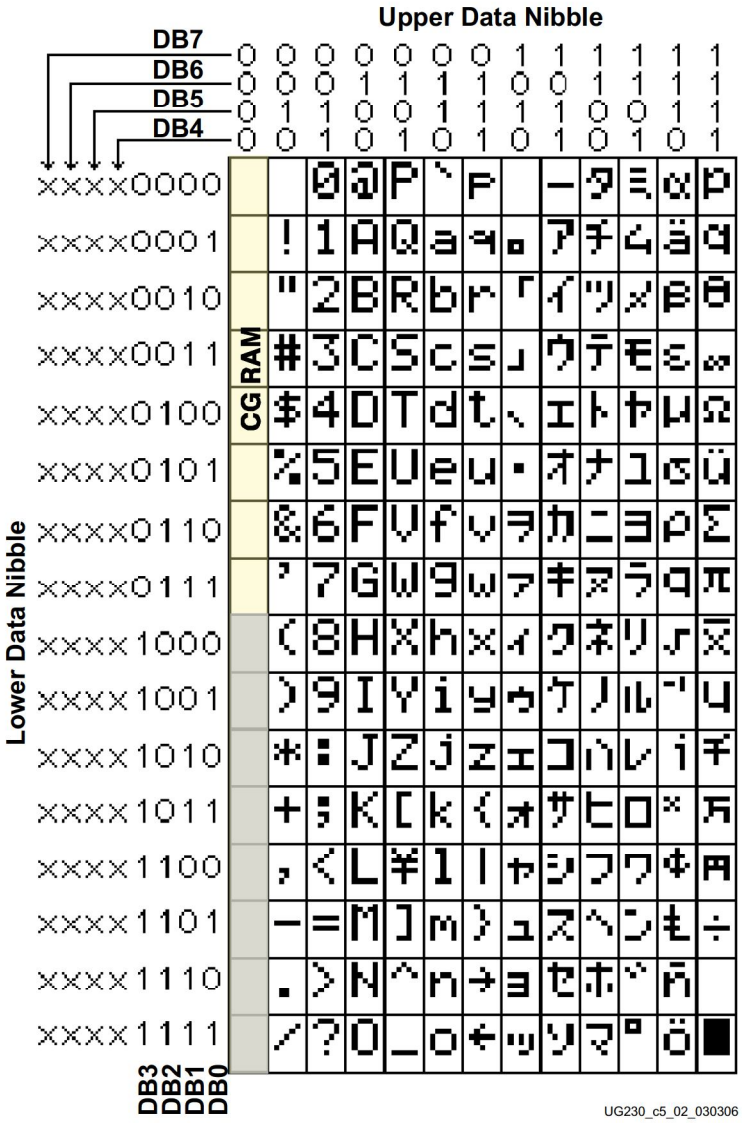

Figure 5-4: **LCD Character Set**

The character ROM contains the ASCII English character set and Japanese katakana characters.

The controller also provides for eight custom character bitmaps, stored in CG RAM. These eight custom characters are displayed by storing character codes 0x00 through 0x07 in a DD RAM location.

CG RAM

The Character Generator RAM (CG RAM) provides space to create eight custom character bitmaps. Each custom character location consists of a 5-dot by 8-line bitmap, as shown in Figure 5-5.

The Set CG RAM Address command initializes the address counter before reading or writing to CG RAM. Write CG RAM data using the Write Data to CG RAM or DD RAM command, and read CG RAM using the Read Data from CG RAM or DD RAM command.

The CG RAM address counter either remains constant after read or write operations, or auto-increments or auto-decrements by one location, as defined by the I/D set by the Entry Mode Set command.

Figure 5-5 provides an example that creates a special *checkerboard* character. The custom character is stored in the fourth CG RAM character location, which is displayed when a DD RAM location is 0x03. To write the custom character, the CG RAM address is first initialized using the Set CG RAM Address command. The upper three address bits point to the custom character location. The lower three address bits point to the row address for the character bitmap. The Write Data to CG RAM or DD RAM command is used to write each character bitmap row. A '1' lights a bit on the display. A '0' leaves the bit unlit. Only the lower five data bits are used; the upper three data bits are *don't care* positions. The eighth row of bitmap data is usually left as all zeros to accommodate the cursor.

						Upper Nibble				Lower Nibble			
						Write Data to CG RAM or DD RAM							
A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Character Address			Row Address			Don't Care			Character Bitmap				
0	1	1	0	0	0	-	-	-	0	■	0	■	0
0	1	1	0	0	1	-	-	-	■	0	■	0	■
0	1	1	0	1	0	-	-	-	0	■	0	■	0
0	1	1	0	1	1	-	-	-	■	0	■	0	■
0	1	1	1	0	0	-	-	-	0	■	0	■	0
0	1	1	1	0	1	-	-	-	■	0	■	0	■
0	1	1	1	1	0	-	-	-	0	■	0	■	0
0	1	1	1	1	1	-	-	-	0	0	0	0	0

Figure 5-5: **Example Custom Checkerboard Character with Character Code 0x03**

Command Set

Table 5-2 summarizes the available LCD controller commands and bit definitions. Because the display is set up for four-bit operation, each eight-bit command is sent as two four-bit nibbles. The upper nibble is transferred first, followed by the lower nibble.

Table 5-2: **LCD Character Display Command Set (4-bit mode)**

Function	LCD_RS	LCD_RW	Upper Nibble				Lower Nibble			
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Clear Display	0	0	0	0	0	0	0	0	0	1
Return Cursor Home	0	0	0	0	0	0	0	0	1	-
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S
Display On/Off	0	0	0	0	0	0	1	D	C	B
Cursor and Display Shift	0	0	0	0	0	1	S/C	R/L	-	-

Table 5-2: **LCD Character Display Command Set (4-bit mode) *(Continued)***

Function	LCD_RS	LCD_RW	Upper Nibble				Lower Nibble			
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Function Set	0	0	0	0	1	0	1	0	-	-
Set CG RAM Address	0	0	0	1	A5	A4	A3	A2	A1	A0
Set DD RAM Address	0	0	1	A6	A5	A4	A3	A2	A1	A0
Read Busy Flag and Address	0	1	BF	A6	A5	A4	A3	A2	A1	A0
Write Data to CG RAM or DD RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Read Data from CG RAM or DD RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Disabled

If the LCD_E enable signal is Low, all other inputs to the LCD are ignored.

Clear Display

Clears the display and returns the cursor to the home position, the top-left corner.

This command writes a blank space (ASCII/ANSI character code 0x20) into all DD RAM addresses. The address counter is reset to 0, location 0x00 in DD RAM. Clears all option settings. The I/D control bit is set to 1 (increment address counter mode) in the Entry Mode Set command.

Execution Time: 82 µs – 1.64 ms

Return Cursor Home

Returns the cursor to the home position, the top-left corner. DD RAM contents are unaffected. Also returns the display being shifted to the original position, shown in Figure 5-3.

The address counter is reset to 0, location 0x00 in DD RAM. The display is returned to its original status if it was shifted. The cursor or blink move to the top-left character location.

Execution Time: 40 µs – 1.6 ms

Entry Mode Set

Sets the cursor move direction and specifies whether or not to shift the display.

These operations are performed during data reads and writes.

Execution Time: 40 µs

Bit DB1: (I/D) Increment/Decrement

0	Auto-decrement address counter. Cursor/blink moves to left.
1	Auto-increment address counter. Cursor/blink moves to right.

This bit either auto-increments or auto-decrements the DD RAM and CG RAM address counter by one location after each Write Data to CG RAM or DD RAM command or Read

Data from CG RAM or DD RAM command. The cursor or blink position moves accordingly.

Bit DB0: (S) Shift

0	Shifting disabled
1	During a DD RAM write operation, shift the entire display value in the direction controlled by Bit DB1 (I/D). It appears as though the cursor position remains constant and the display moves.

Display On/Off

The display is turned on or off, controlling all characters. The cursor and cursor position character (underscore) blink.

Execution Time: 40 µs

Bit DB2: (D) Display On/Off

0	No characters displayed. However, data stored in DD RAM is retained.
1	Display characters stored in DD RAM

Bit DB1: (C) Cursor On/Off

The cursor uses the five dots on the bottom line of the character. The cursor appears as a line under the displayed character.

0	No cursor
1	Display cursor

Bit DB0: (B) Cursor Blink On/Off

0	No cursor blinking
1	Cursor blinks on and off approximately every half second

Cursor and Display Shift

Moves the cursor and shifts the display without changing DD RAM contents. Shift cursor position or display to the right or left without writing or reading display data.

This function positions the cursor in order to modify an individual character, or to scroll the display window left or right to reveal additional data stored in the DD RAM, beyond the 16th character on a line. The cursor automatically moves to the second line when it shifts beyond the 40th character location of the first line. The first and second line displays shift at the same time.

When the displayed data is shifted repeatedly, both lines move horizontally. The second display line does not shift into the first display line.

Execution Time: 40 µs

Table 5-3: **Shift Patterns According to S/C and R/L Bits**

DB3 (S/C)	DB2 (R/L)	Operation
0	0	Shift the cursor position to the left. The address counter is decremented by one.
0	1	Shift the cursor position to the right. The address counter is incremented by one.
1	0	Shift the entire display to the left. The cursor follows the display shift. The address counter is unchanged.
1	1	Shift the entire display to the right. The cursor follows the display shift. The address counter is unchanged.

Function Set

Sets the interface data length, the number of display lines, and the character font.

The Starter Kit board supports a single function set with value 0x28.

Execution Time: 40 µs

Set CG RAM Address

Sets the initial CG RAM address.

After this command, all subsequent read or write operations to the display are to or from CG RAM.

Execution Time: 40 µs

Set DD RAM Address

Sets the initial DD RAM address.

After this command, all subsequent read or write operations to the display are to or from DD RAM. The addresses for displayed characters appear in Figure 5-3.

Execution Time: 40 µs

Read Busy Flag and Address

Reads the Busy flag (BF) to determine if an internal operation is in progress, and reads the current address counter contents.

BF = 1 indicates that an internal operation is in progress. The next instruction is not accepted until BF is cleared or until the current instruction is allowed the maximum time to execute.

This command also returns the present value of the address counter. The address counter is used for both CG RAM and DD RAM addresses. The specific context depends on the most recent Set CG RAM Address or Set DD RAM Address command issued.

Execution Time: 1 µs

Write Data to CG RAM or DD RAM

Writes data into DD RAM if the command follows a previous Set DD RAM Address command, or writes data into CG RAM if the command follows a previous Set CG RAM Address command.

After the write operation, the address is automatically incremented or decremented by 1 according to the Entry Mode Set command. The entry mode also determines display shift.

Execution Time: 40 µs

Read Data from CG RAM or DD RAM

Reads data from DD RAM if the command follows a previous Set DD RAM Address command, or reads data from CG RAM if the command follows a previous Set CG RAM Address command.

After the read operation, the address is automatically incremented or decremented by 1 according to the Entry Mode Set command. However, a display shift is not executed during read operations.

Execution Time: 40 µs

Operation

The board has an eight-bit data interface to the character LCD. Other Xilinx boards use a four-bit interface. As shown in Figure 5-1, the Spartan-3A/3AN Starter Kit board supports both an eight-bit and a four-bit interface for compatibility reasons. Many existing reference designs are already built around a four-bit interface.

Four-Bit Data Interface

Figure 5-6 illustrates a write operation to the LCD, showing the minimum times allowed for setup, hold, and enable pulse length relative to the 50 MHz clock (20 ns period) provided on the board.

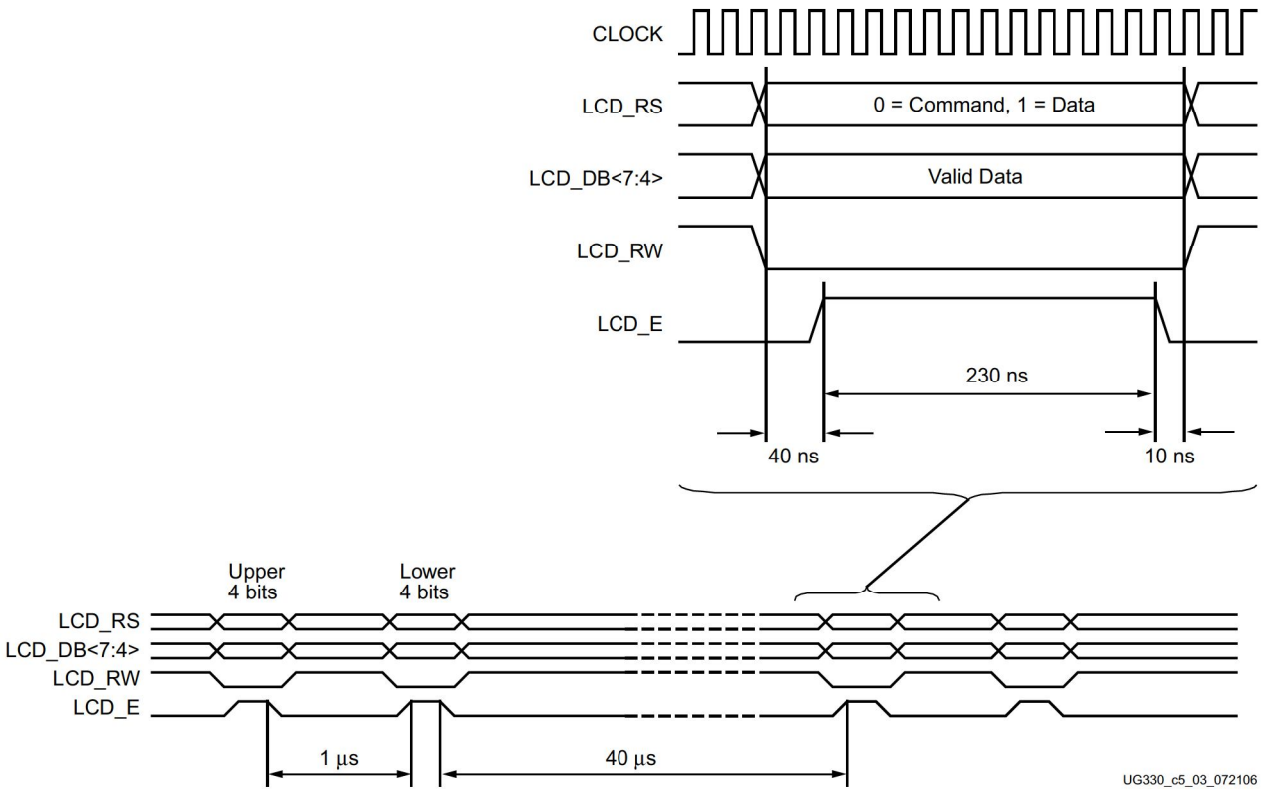

Figure 5-6: **Character LCD Interface Timing**

The data values on LCD_DB<7:4>, and the register select (LCD_RS) and the read/write (LCD_RW) control signals must be set up and stable at least 40 ns before the enable LCD_E goes High. The enable signal must remain High for 230 ns or longer—the equivalent of 12 or more clock cycles at 50 MHz.

In many applications, the LCD_RW signal can be tied Low permanently because the FPGA generally has no reason to read information from the display.

Transferring Eight-Bit Data over the Four-Bit Interface

After initializing the display and establishing communication in four-bit mode, all commands and data transfers to the character display are via eight bits, transferred using two sequential four-bit operations. Each eight-bit transfer must be decomposed into two four-bit transfers, spaced apart by at least 1 µs, as shown in Figure 5-6. The upper nibble is transferred first, followed by the lower nibble. An eight-bit write operation must be spaced least 40 µs before the next communication. This delay must be increased to 1.64 ms following a Clear Display command.

~~Initializing the Display~~

~~After power-on, the display must be initialized to establish the required communication protocol. The initialization sequence is simple and ideally suited to the highly efficient eight bit PicoBlaze embedded controller. After initialization, the PicoBlaze controller is available for more complex control or computation beyond simply driving the display.~~